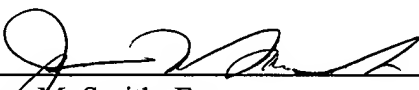


REMARKS

The amendments to the specification are being made to correct typographical errors.

Respectfully submitted,

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MARKED UP VERSION OF AMENDMENTS

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Specification Amendments Under 37 C.F.R. § 1.121(b)(1)(iii)

Replace the paragraph at page 2, line 23 through page 3, line 2 with the below paragraph marked up by way of bracketing and underlining to show the changes relative to the previous version of the paragraph.

A digital cross connect can be implemented in a straightforward manner by demultiplexing each input port, switching all of the time slots of all of the input ports with a space switch, and then multiplexing each output port. This approach is illustrated in Figure 2. The four time slots of input port 1 are demultiplexed (Demux) in demultiplexers 32 so that each is carried on a separate line. All of these demultiplexed lines are then switched by a space switch 34 to the appropriate output time slots. Finally, a set of multiplexers (Mux) 36 multiplexes the time slots of each output channel onto each output port. This approach is used, for example, in the systems described in U.S. Patents [3,735,409] 3,735,049 and 4,967,405.

Replace the paragraph at page 3, lines 11 through 19 with the below paragraph marked up by way of bracketing and underlining to show the changes relative to the previous version of the paragraph.

A more economical digital cross connect can be realized using a time-space-time (T-S-T) switch architecture as illustrated in Figure 3. Here each input port is input to a time-slot interchanger (TSI) 38. A TSI switches a multiplexed input stream in time by interchanging the positions of the time slots. To switch time-slot i to time-slot j, for example, slot i is delayed by  $T+j-i$  byte times. The multiplexed streams out of the input TSIs are then switched by a  $P \times P$  space switch 40 that is reconfigured on each time slot. The outputs of this space switch are switched in time again by a set of output TSIs 42. This T-S-T architecture is employed, for example, by the systems described in U.S. Patents 3,736,381 and [3,927,467] 3,927,267.